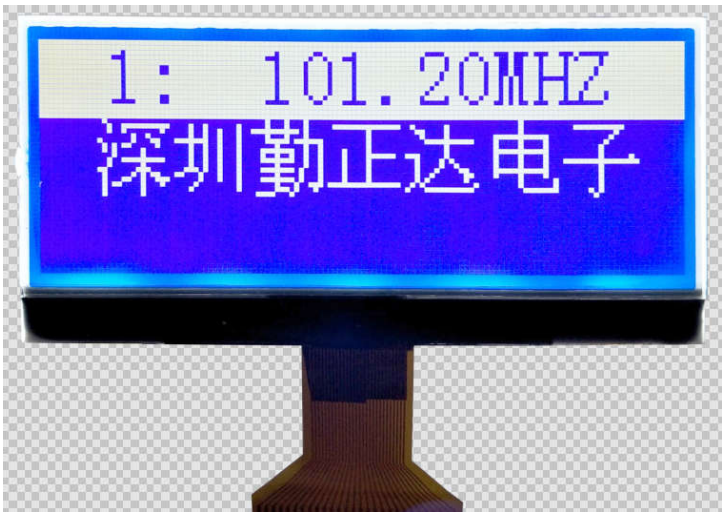
图形点阵液晶显示屏使用手册

FM13248



深圳市勤正达电子有限公司

地址:深圳市龙华区大浪街道华宁路颐丰华产业园创客中心 2 楼
电话：0755-81798090
传真：0755-81798636

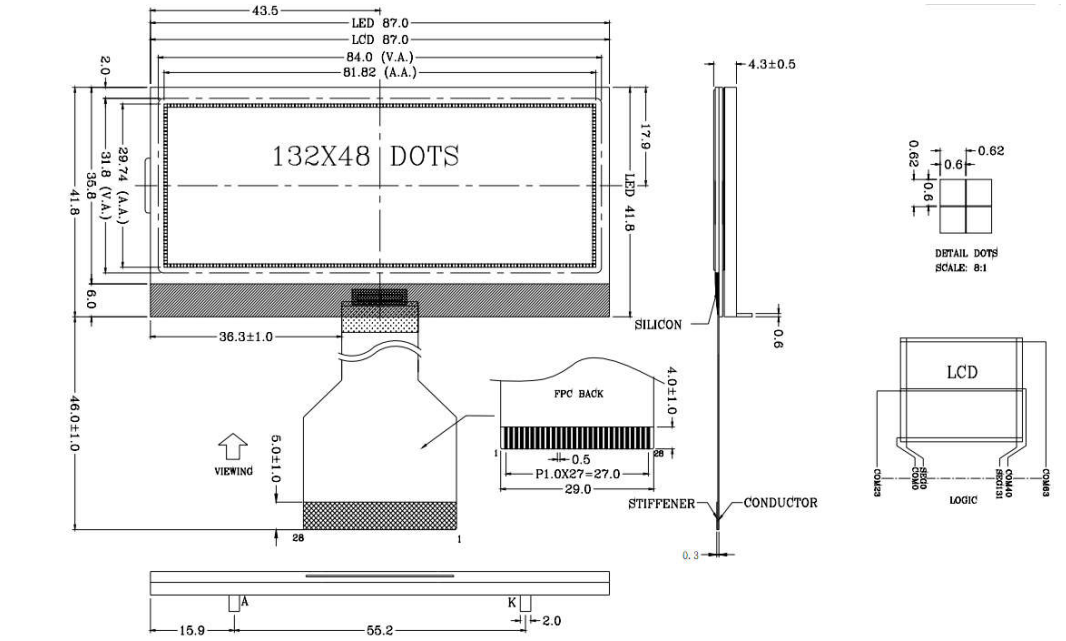
一.概述：

FM13248 是一款图形点阵液晶显示器。它主要采用动态驱动原理由 NT7534 图形控制器对 132(列)×48(行)的全点控制并驱动显示。此显示器采用了 COG 的封装方式,使其寿命长，连接可靠。

二.特性：

Construction	:	COG+FPC
Display Format	:	132x48 dots
Display Type	:	STN, Transmissive, Negative, Blue
Controller	:	NT7534 or equivalent controller
Interface	:	8-bit parallel interface
Backlight	:	white/ side light
Viewing Direction	:	6 O’clock
Driving Scheme	:	1/49 Duty Cycle, 1/8 Bias
Power Supply Voltage	:	3.0 V
VLCD Supply Voltage	:	9.0 V (VOP.)
Operation temperature	:	-20℃ to +70℃
Storage temperature	:	-30℃ to +80℃

三.外形尺寸：



NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
DEF.	/CS1	/RES	A0	RW_WR	E_RD	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	VDD	VSS	VOUT	C3+	C1-	C1+	C2+	C2-	V1	V2	V3	V4	V0	CS2	P/S

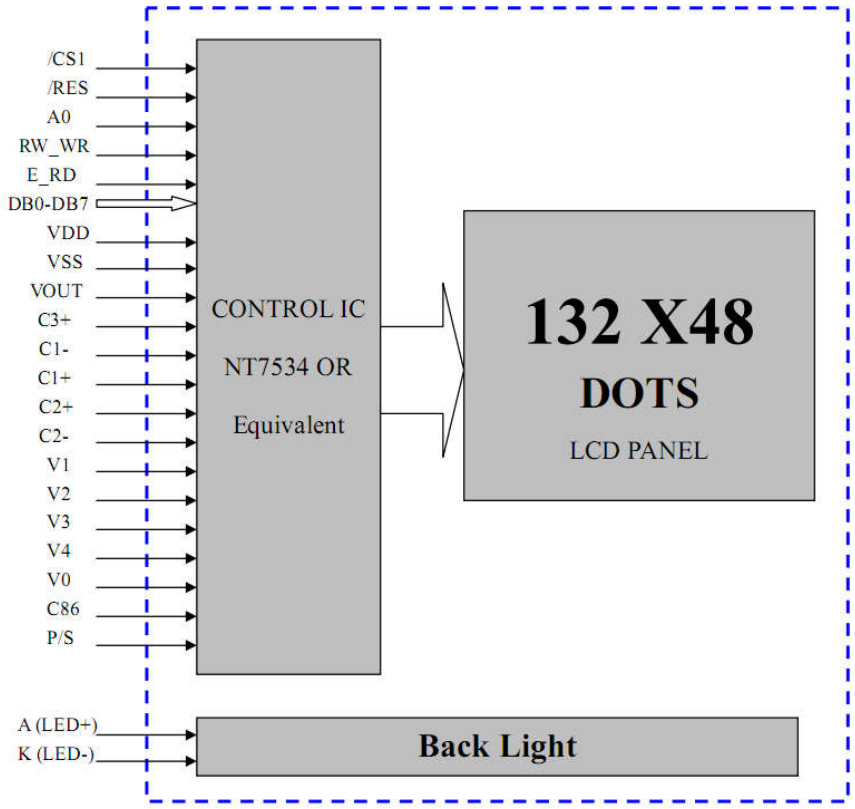
四.硬件说明

1.引脚特性

引脚号	引脚名称	级　别	引　　脚　　功　　能　　描　　述
1	/CS	H/L	片选。L：选择
2	/RES	H/L	复位，L：复位。
3	A0	H/L	寄存器选择。H：数据。L：命令
4	/WR (R/W)	H/L	8080 :低电平有效。在数据总线上的信号在/WR 信号的上升沿被锁存。 6800 MPU 的访问类型,并决定： 当 R/W =“H”：读。 当 R/W =“L”：写。
5	RD(E)	H/L	6800 时序：使能。H：写使能。L 读使能。 8080 时序：H:无效。L：读数据。
6	DB0	H/L	8位双向数据总线连接到一个8位或16位标准 MPU 数据总线。 选择当串行接口（SPI）(P/S =“L”)： D7：串行数据输入（SI)； D6：串行时钟输入（SCL)。 D0到 D5应连接到 VDD 或浮动。
7	DB1		
8	DB2		
9	DB3		
10	DB4		
11	DB5		
12	DB6 （SCL）		
13	DB7 (SI)		
14	VDD	+3.0V	电源
15	VSS	0V	电源地
16	VOUT	--	连接一个电容(1.0uF-4.7uF),此终端与 VSS 或 VDD 相连
17	C3+	--	连接一个电容(1.0uF-4.7uF),此端子与 C1-相连
18	C1-	--	连接一个电容(1.0uF-4.7uF),此端子与 C1+和 C3+相连
19	C1+	--	连接一个电容(1.0uF-4.7uF),此端子与 C1-相连
20	C2+	--	连接一个电容(1.0uF-4.7uF),此端子与 C2-相连
21	C2-	--	连接一个电容(1.0uF-4.7uF),此端子与 C2+相连
22	V1	--	连接一个电容(0.1uF-2.2uF),此端子与 VSS 或 VDD 相连

23	V2	--	连接一个电容(0.1uF-2.2uF),此端子与 VSS 或 VDD 相连
24	V3	--	连接一个电容(0.1uF-2.2uF),此端子与 VSS 或 VDD 相连
25	V4	--	连接一个电容(0.1uF-2.2uF),此端子与 VSS 或 VDD 相连
26	V0	--	连接一个电容(0.1uF-2.2uF),此端子与 VSS 或 VDD 相连
27	C86	H/L	MPU 接口选择引脚。(P/S=“H”) C86 =“H”: 6800系列 MPU 接口; C86 =“L”: 8080系列 MPU 接口。
28	P/S	H/L	引脚可配置的接口是并行模式或串行模式。 P/S =“H”: 输入/输出的并行数据; P/S =“L”: 串行数据输入。 当 P/S =“L”时,必须固定 D0到 D5为“ H”。 /RD(E)和/ WR(R/W)被固定为“H”或“L”. 串行存取模式不支持读操作

2. 原理简图



五.电气特性

1.限定参数

项　　目	名称	值	单位	备 注
Operating Voltage	VDD	+3.0	V	*1
Supply Voltage	VEE	VDD-3.3toVDD-3.0	V	*2

项　　目	名称	值	单位	备 注
Operating Temperature	T_{OPR}	-20 to +70	℃	
Storage Temperature	T_{STG}	-30 to +80	℃	

*1.Based on VSS=0V
*2.Applies to V_{LCD}

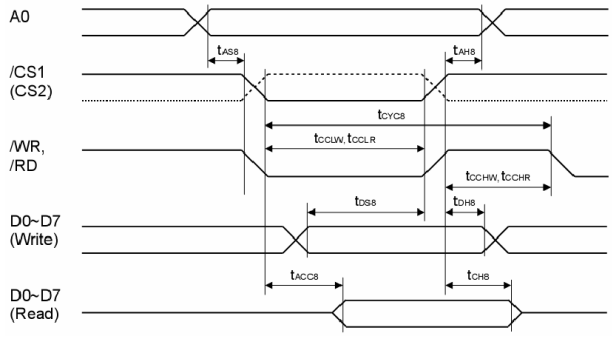
2.直流特性（VDD=+3.0V，VSS=0V，VLCD=9.0V，Ta=-20～+70℃）

项　　目	名称	测试条件	Min	Typ	Max	单位	备注
Input High Voltage	V_{IH}	-	2.4	-	VDD	V	*1
Input Low Voltage	V_{IL}	-	0	-	0.6	V	*1
Output High Voltage	V_{OH}	I_{OH}=-500uA	2.4	-	-	V	*2
Output Low Voltage	V_{OL}	I_{OL}=0.5mA		-	0.6	V	*2
Input Leakage Current	I_{LKG}	V_{IN}=VSS～VDD	-1.0	-	1.0	uA	*3
Three-state(OFF) input Current	I_{TSL}	V_{IN}=VSS～VDD	-3.0	-	3.0	uA	*4
Operating Current	I_{DD1}	During Display	-	-	0.5	mA	*5
	I_{DD2}	During Access			1	mA	*5

*1.CS,E,RW,A0,DB0～DB7
*2.DB0～DB7
*3.Except DB0～DB7
*4.DB0～DB7 at High Impedance
*5.1/49 duty，Output：NO Load

六.MPU 时序图

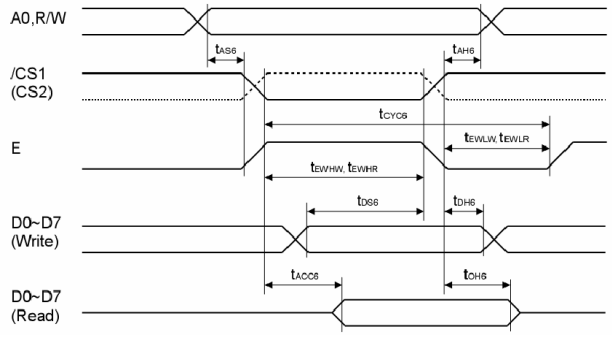
1.8080 系列 MPU 时序图:



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{AH8}	Address hold time	0	-	-	ns	A0
T_{AS8}	Address setup time	0	-	-	ns	
t_{CYC8}	System cycle time	240	-	-	ns	
t_{CCLW}	Control low pulse width (write)	90	-	-	ns	/WR
t_{CCLR}	Control low pulse width (read)	120	-	-	ns	/RD
t_{CCHW}	Control high pulse width (write)	100	-	-	ns	/WR
t_{CCHR}	Control high pulse width (read)	60	-	-	ns	/RD
T_{DS8}	Data setup time	40	-	-	ns	D0~D7
T_{DH8}	Data hold time	10	-	-	ns	
t_{ACC8}	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
T_{CH8}	Output disable time	5	-	50	ns	

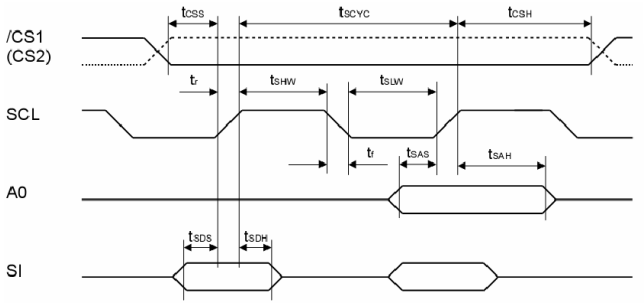
2. 6800 系列 MPU 时序图:



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH6}	Address hold time	0	-	-	ns	A0, R/W
t_{AS6}	Address setup time	0	-	-	ns	
t_{CYC6}	System cycle time	240	-	-	ns	
t_{EWHW}	Control high pulse width (write)	90	-	-	ns	E
t_{EWHR}	Control high pulse width (read)	120	-	-	ns	E
t_{EWLW}	Control low pulse width (write)	100	-	-	ns	E
t_{EWLR}	Control low pulse width (read)	60	-	-	ns	E
t_{DS6}	Data setup time	40	-	-	ns	D0~D7
t_{DH6}	Data hold time	10	-	-	ns	
t_{ACC6}	/RD access time	-	-	140	ns	D0~D7 CL = 100pF
t_{OH6}	Output disable time	5	-	50	ns	

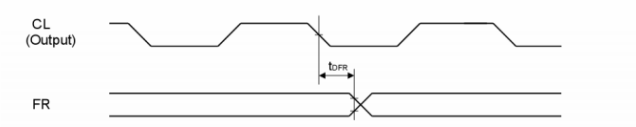
3. SPI 系列 MPU 时序图



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	120	-	-	ns	SCL
t_{SHW}	Serial clock H pulse width	60	-	-	ns	SCL
t_{SLW}	Serial clock L pulse width	60	-	-	ns	SCL
t_{SAS}	Address setup time	30	-	-	ns	A0
t_{SAH}	Address hold time	20	-	-	ns	A0
t_{SDS}	Data setup time	30	-	-	ns	SI
t_{SDH}	Data hold time	20	-	-	ns	SI
t_{CSS}	Chip select setup time	20	-	-	ns	/CS1, CS2
t_{CSH}	Chip select hold time	40	-	-	ns	/CS1, CS2

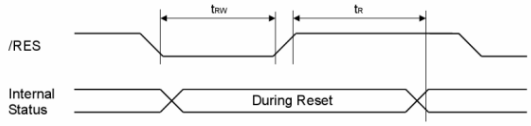
4. Display Control Timing



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{DFR}	FR delay time	-	20	80	ns	CL = 50 pF

5. Reset Timing



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset Time	-	-	1.0	µs	
t_{RW}	Reset low pulse width	10	-	-	µs	/RES

七. 指令列表：

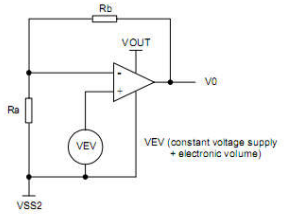
Command	A0	/RD	/WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when high, and turn off when low
(2) Display Start Line Set	0	1	0	0	1	Display Start Address						40h to 7Fh	Specifies RAM display line for COM0
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				B0h to B8h	Set the display data RAM page in Page Address register
(4) Column Address Set	0	1	0	0	0	0	1	Higher Column Address				00h to 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower Column Address					
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low, but full indication when high
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Select normal display (0) or entire display on
(11)LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15)Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Select COM output scan direction *: invalid data
(16)Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Select the power circuit operation mode
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Select internal resistor ratio Rb/Ra mode
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
(19)Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation

Command	A0	/RD	/WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(22)Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Select the oscillation frequency
(23)Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0 1	82h 83h	Enter/Release the partial display mode
(24)Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode
(25)Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode
(26)Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set
Partial Start Line Set	0	1	0	1	1	Partial Start Line						XX	Sets the LCD Number of partial display start line
(27)N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion
Number of Line Set	0	1	0	*	*	*	Number of Line					XX	Sets the number of line used for N-Line inversion
(28)N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion
(29)DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division				XX	Set the Division of DC/DC Clock Frequency
(30)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(31)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

Note: Do not use any other command, or system malfunction may result.

八．对比度设置：

$$V0 = (1+\frac{Rb}{Ra}) \times VEV = (1+\frac{Rb}{Ra}) \times (1-\frac{63-\alpha}{162}) \times VREG \qquad \text{(Equation A-1)}$$



VREG is the IC internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 10.

Table 10

Equipment Type	Thermal Gradient	Units	VREG
Internal Power Supply	-0.05	%/°C	2.1

D5	D4	D3	D2	D1	D0	α	V0
0	0	0	0	0	0	0	Minimum
0	0	0	0	0	1	1	:
0	0	0	0	1	0	2	:
		:			:	:	:
1	0	0	0	0	0	32	(default)
		:			:	:	:
1	1	1	1	1	0	62	:
1	1	1	1	1	1	63	Maximum

V0 voltage regulator internal resistance ratio register value and (1+ Rb/Ra) ratio (Reference value)

Register			Equipment Type by Thermal Gradient [Units:%/°C]
D2	D1	D0	-0.05
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0 (default)
1	0	1	5.5
1	1	0	6.0
1	1	1	6.4