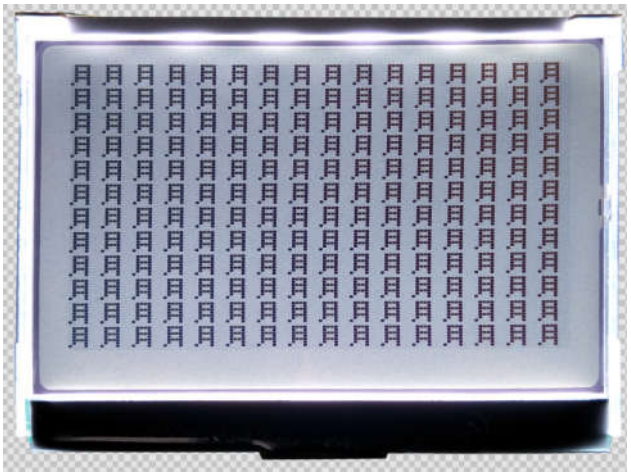
图形点阵液晶显示模块使用手册

FM12896C



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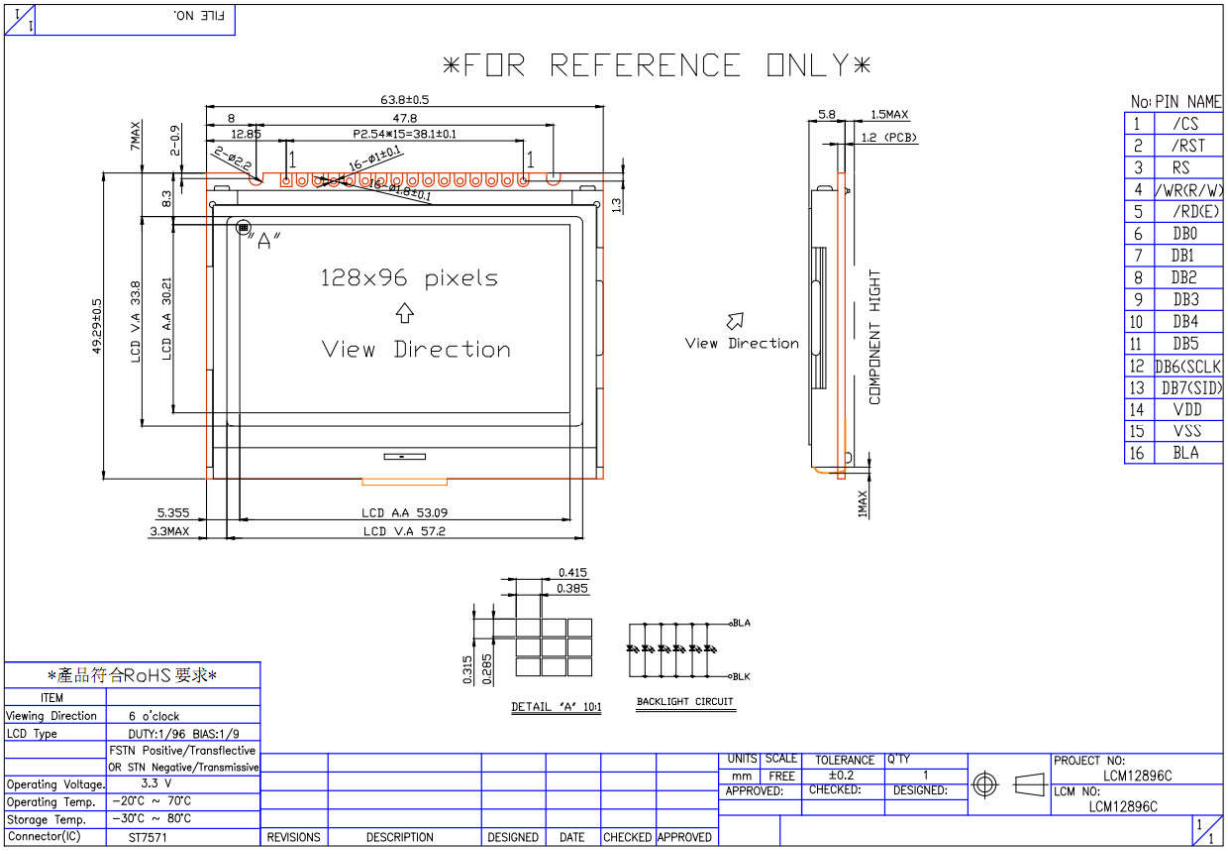
一. 概述

FM12896C 是一种图形点阵液晶显示器。它主要采用动态驱动原理由 ST7571 图形控制器对 128(列)×96(行)的全点控制并驱动显示。此显示器采用了 COG 的封装方式加 PCB 板结构,使其寿命长，连接可靠。

1. 工作电压为+3.3V ,内建升压器，电压跟随器，对比度调节。
2. 全屏幕点阵，点阵数为 128(列)×96(行),可显示 8(列)×6(行)个(16×16 点阵)汉字，也可完成图形，字符的显示。
3. 与 CPU 接口可选择 4 种控制方式，分别为：6800 模式、8080 模式、4-SPI 模式、3-SPI 模式。默认 4-SPI 系列时序。
4. 简单的操作指令。

二. 外形尺寸

1. 外形尺寸图：



2.主要外形尺寸

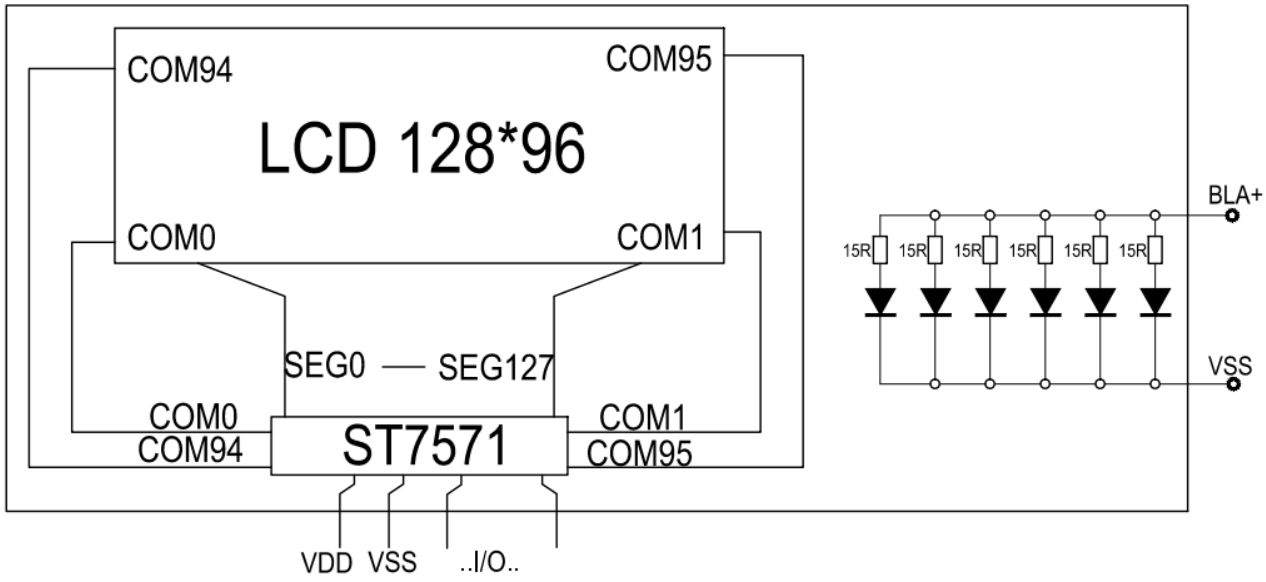
项　　目	标　准　尺　寸	单　　位
模　块　体　积	63.80×49.29×5.8	mm
视　　域	57.2×33.8	mm
行 列 点 阵 数	128×96	dots
点　　距　　离	0.415×0.315	mm
点　　大　　小	0.385×0.285	mm

三.硬件说明

1.引脚特性

引脚号	引脚名称	级　别	引　　脚　　功　　能　　描　　述
1	/CS	H/L	片选,L：选择
2	/RST	H/L	复位，L：复位。
3	RS	H/L	寄存器选择,H：数据。L：命令
4	/WR(R/W)	H/L	8080 :低电平有效。在数据总线上的信号在/WR 信号的上升沿被锁存。 6800 MPU 的访问类型,并决定： 当 R/W =“H”：读。 当 R/W =“L”：写。
5	/RD(E)	H/L	6800 时序：使能。H：写使能。L 读使能。 8080 时序：H:无效。L：读数据。
6	DB0	H/L	8位双向数据总线连接到一个8位或16位标准 MPU 数据总线。 选择当串行接口（SPI)： DB7：串行数据输入（SID)； DB6：串行时钟输入（SCLK)。 DB0 到 DB5 应连接到 VDD 或浮动。
7	DB1	H/L	
8	DB2	H/L	
9	DB3	H/L	
10	DB4	H/L	
11	DB5	H/L	
12	DB6(SLCK)	H/L	
13	DB7(SID)	H/L	
14	VDD	+3.3V	电源正极
15	VSS	0V	电源负极
16	BLA+	+3.3V	背光电源正极

2.原理简图



四.电气特性

1.限定参数

项　　目	名称	值	单位	备 注
Operating Voltage	VDD	+3.0 to +3.3	V	*1
Supply Voltage	VEE	VDD-3.3toVDD-3.0	V	*2

项　　目	名称	值	单位	备 注
Operating Temperature	T_{OPR}	-20 to +70	℃	
Storage Temperature	T_{STG}	-30 to +80	℃	

*1.Based on VSS=0V
*2.Applies to V_{LCD}

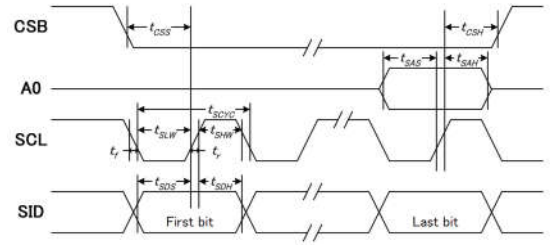
2.直流特性（VDD=+3.3V％, VSS=0V, VLCD=9.5V, Ta=-20～+70℃）

项　　目	名称	测试条件	Min	Typ	Max	单位	备注
Input High Voltage	V_{IH}	-	2.4	-	VDD	V	*1
Input Low Voltage	V_{IL}	-	0	-	0.6	V	*1
Output High Voltage	V_{OH}	I_{OH}=-500uA	2.4	-	-	V	*2
Output Low Voltage	V_{OL}	I_{OL}=0.5mA		-	0.6	V	*2
Input Leakage Current	I_{LKG}	V_{IN}=VSS～VDD	-1.0	-	1.0	uA	*3
Three-state(OFF) input Current	I_{TSL}	V_{IN}=VSS～VDD	-3.0	-	3.0	uA	*4
Operating Current	I_{DD1}	During Display	-	-	0.5	mA	*5
	I_{DD2}	During Access			1	mA	*5

*1.CSB,A0,SCLK、SID.　*2.SCLK、SID.　*3.Except SCLK、SID
*4.SCLK、SID at High Impedance.　*5.1/96 duty, Output: NO Load

3. 时序特性：

4-SPI(PCB 背面短接 JP1、JP4)：

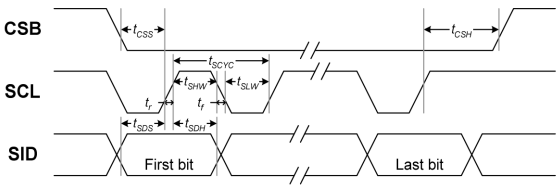


(VDD1 = 1.8V~3.3V, Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SID	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

- The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
- All timing is specified using 20% and 80% of VDD1 as the standard.

3-SPI(PCB 背面短接 JP3、JP4)：

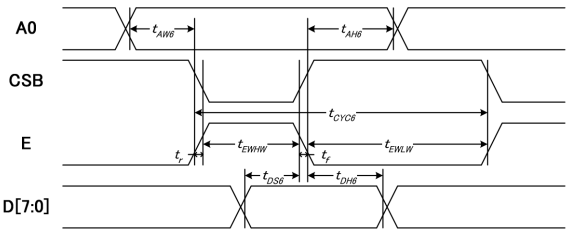


(VDD1 = 1.8V~3.3V, Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Data setup time	SID	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

- The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
- All timing is specified using 20% and 80% of VDD1 as the standard.

6800 模式(PCB 背面短接 JP1、JP2)：

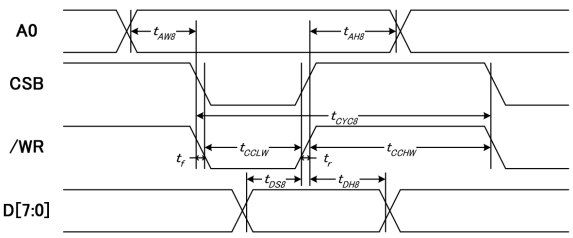


(VDD1 = 1.8V~3.3V, Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time	E	tCYC6		500	—	
Enable L pulse width (Write)		tEWLW		250	—	
Enable H pulse width (Write)		tEWHW		250	—	
WRITE Data setup time	DB[7:0]	tDS6		80	—	
WRITE Data hold time		tDH6		30	—	

- The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 – tEWLW – tEWHW) is specified.
- All timing is specified using 20% and 80% of VDD1 as the reference.
- tEWLW is specified as the overlap between CSB being "H" and E being "L".
- R/W signal is always "H".

8080 模式(PCB 背面短接 JP2、JP3)：



(VDD1 = 1.8V~3.3V, Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time	/WR	tCYC8		500	—	
Write L pulse width		tCCLW		250	—	
Write H pulse width		tCCHW		250	—	
WRITE Data setup time	DB[7:0]	tDS8		80	—	
WRITE Data hold time		tDH8		30	—	

- The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) is specified.
- All timing is specified using 20% and 80% of VDD1 as the reference.
- tCCLW is specified as the overlap between CSB being "L" and /WR being at the "L" level.

Reset Timing

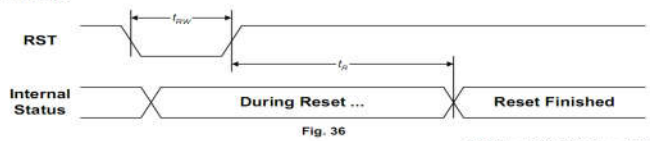


Fig. 36

(VDD1 = 1.8V~3.3V, Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Units
Reset time		tR		120	—	—	ms
Reset "L" pulse width	RST	tRW		2.0	—	—	us

4. 命令设置：

Instruction	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Section
Set Mode	0	0	0	0	1	1	1	0	0	0	2-byte instruction FR[3:0]: Set frame frequency BE[1:0]: Set booster efficiency	9.1.1
	0	0	FR3	FR2	FR1	FR0	BE1	BE0	--	0		
Write Display Data	1	0	Write data								Write data into DDRAM	9.1.2
Set Icon	0	0	1	0	1	0	0	0	1	ION	ION=0: Disable Icon function ION=1: Enable Icon function and set Page Address = 16	9.1.3
Set Page Address	0	0	1	0	1	1	P3	P2	P1	P0	Set Page Address	9.1.4
Set Column Address (MSB)	0	0	0	0	0	1	0	X7	X6	X5	Set MSB of Column Address	9.1.5
Set Column Address (LSB)	0	0	0	0	0	0	X4	X3	X2	X1	Set LSB of Column Address	9.1.6
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: Display OFF D=1: Display ON	9.1.7
Set Display Start Line	0	0	0	1	0	0	0	0	--	--	2-byte instruction. Specify Line Address for the 1st display line of DDRAM (vertical scrolling).	9.1.8
	0	0	--	S6	S5	S4	S3	S2	S1	S0		
Set COM0	0	0	0	1	0	0	0	1	--	--	2-byte instruction. Specify a COM pin to be COM0 (moving partial display window).	9.1.9
	0	0	--	C6	C5	C4	C3	C2	C1	C0		
Set Display Duty	0	0	0	1	0	0	1	0	--	--	2-byte instruction. Set display duty	9.1.10
	0	0	L7	L6	L5	L4	L3	L2	L1	L0		
Set N-line Inversion	0	0	0	1	0	0	1	1	--	--	2-byte instruction. Set N-line inversion counter	9.1.11
	0	0	--	--	--	N4	N3	N2	N1	N0		
Release N-line Inversion	0	0	1	1	1	0	0	1	0	0	Exit N-line inversion mode	9.1.12
Reverse Display	0	0	1	0	1	0	0	1	1	REV	REV=0: Normal display REV=1: Reverse display	9.1.13
Entire Display ON	0	0	1	0	1	0	0	1	0	EON	EON=0: Normal display EON=1: Entire display ON	9.1.14

Instruction	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Section
Power Control	0	0	0	0	1	0	1	VC	VR	VF	Set internal power ON/OFF	9.1.15
Select Regulator Register	0	0	0	0	1	0	0	R2	R1	R0	Select internal Regulator resistor	9.1.16
Set Contrast	0	0	1	0	0	0	0	0	0	1	2-byte instruction. Select EV for internal Regulator's reference	9.1.17
	0	0	--	--	EV5	EV4	EV3	EV2	EV1	EV0		
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias	9.1.18
Set COM Scan Direction	0	0	1	1	0	0	MY	--	--	--	Set COM scan direction: MY=0: Normal direction MY=1: Reverse direction	9.1.19
Set SEG Scan Direction	0	0	1	0	1	0	0	0	0	MX	Set SEG scan direction: MX=0: Normal direction MX=1: Reverse direction	9.1.20
Oscillator ON	0	0	1	0	1	0	1	0	1	1	Turn ON internal Oscillator	9.1.21
Set Power-Save Mode	0	0	1	0	1	0	1	0	0	P	P=0: Normal mode P=1: Enable Power-Save mode	9.1.22
Release Power-Save Mode	0	0	1	1	1	0	0	0	0	1	Exit Power-Save mode	9.1.23
RESET	0	0	1	1	1	0	0	0	1	0	Software reset	9.1.24
Set Display Data Length	--	--	1	1	1	0	1	0	0	0	2-byte instruction. Set the data counter in 3-Line SPI only	9.1.25
	--	--	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0		
NOP	0	0	1	1	1	0	0	0	1	1	No operation	9.1.26
Reserved	0	0	1	1	1	0	0	0	0	0	Do NOT use	--
Reserved	0	0	1	1	1	0	1	1	1	0	Do NOT use	--
Reserved	0	0	1	1	1	1	--	--	--	--	Reserved for testing	--
Extension Command Set1	0	0	1	1	1	1	1	1	0	TE1	TE1=1: Enter extension Mode1	9.1.27
Extension Command Set2	0	0	1	1	0	1	0	0	0	TE2	TE2=1: Enter extension Mode2	9.1.28
Extension Command Set3	0	0	0	1	1	1	1	0	1	TE3	TE3=1: Enter extension Mode3	9.1.29

Instruction	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXTENSION COMMAND SET 1											
Increase Vop offset	0	0	0	1	0	1	0	0	0	1	Increase vop offset by 1step
Decrease Vop offset	0	0	0	1	0	1	0	0	1	0	Decrease vop offset by 1 step
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode
EXTENSION COMMAND SET 2											
Disable autoread	0	0	1	0	1	0	1	0	1	0	Disable autoread
Enter EEPROM mode	0	0	0	0	0	1	0	0	1	1	Enter EEPROM mode
Enable read mode	0	0	0	0	1	0	0	0	0	0	Enable read mode
Set read pulse	0	0	0	1	1	1	0	0	0	1	Set read pulse width
Exit EEPROM mode	0	0	1	0	0	0	0	0	1	1	Exit EEPROM mode
Enable erase mode	0	0	0	1	0	0	1	0	1	0	Enable erase mode
Set erase pulse	0	0	0	1	0	1	0	1	0	1	Set erase pulse width
Enable write mode	0	0	0	0	1	1	0	1	0	1	Enable write mode
Set write pulse	0	0	0	1	1	0	1	0	1	0	Set write pulse width
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode
EXTENSION COMMAND SET 3											
Set Color Mode	0	0	0	0	0	1	0	0	0	B/G	Select Black/White or Gray mode B/G=1: Black/White mode; B/G=0: Gray mode (default)
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode

Note: Do NOT use non-specified instructions in any extension command mode.