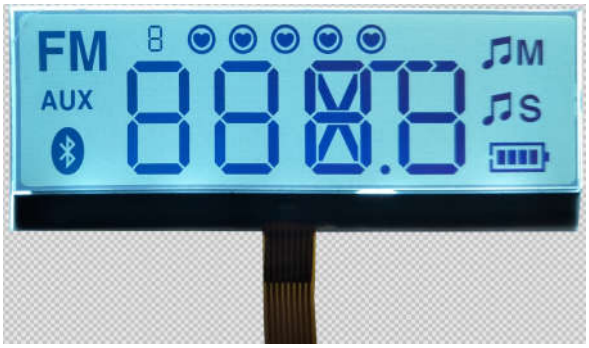
FM-6422 液晶显示屏使用手册



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一. 概述：

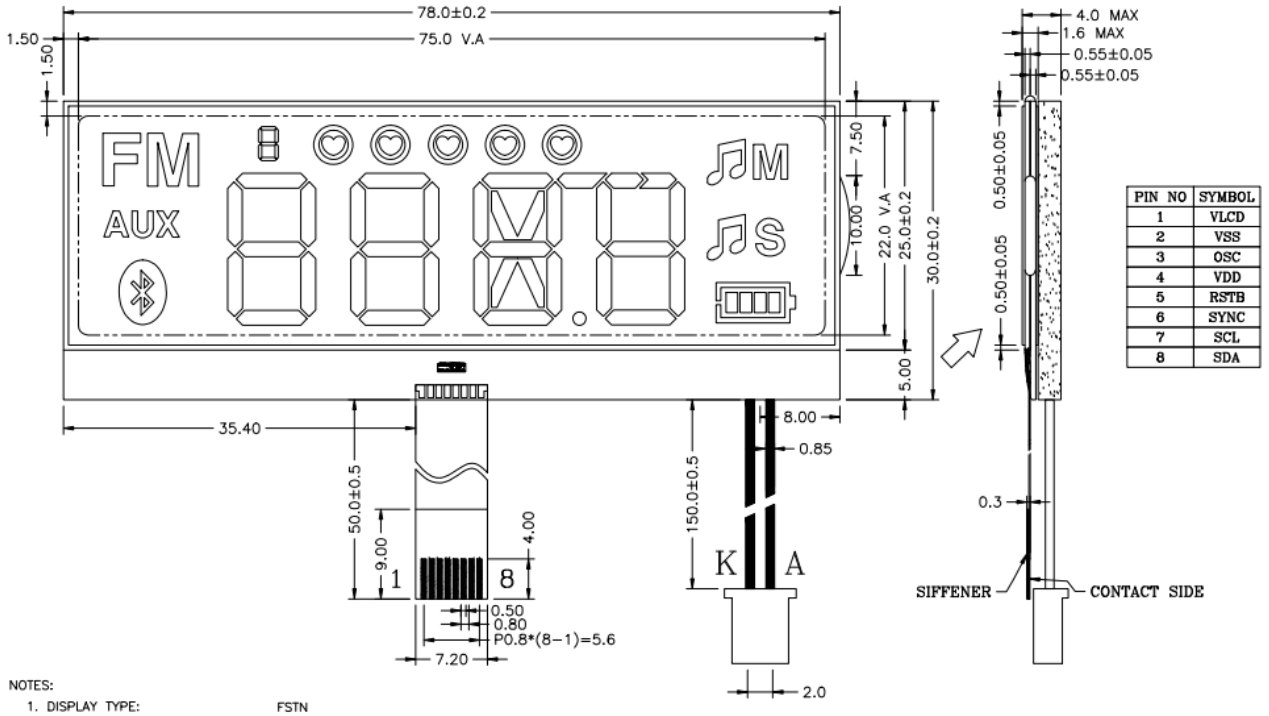
FM-6422 是一款段码型液晶显示屏。它主要采用动态驱动原理由 UC1671C 控制器对段码进行控制并驱动显示。此显示器采用了 COG 加 FPC 的封装方式,使其寿命长，连接可靠。

二. 特性：

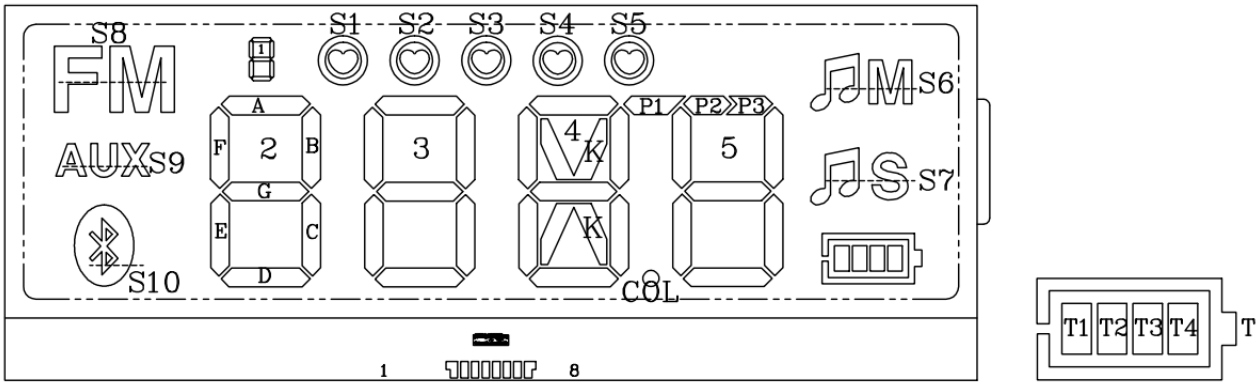
1. 工作电压为+5.0V。
2. 与 CPU 接口采用 IIC 总线协议。

三. 外形尺寸：

1. 外形结构图:



2.逻辑图:



COM \ SEG	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13
COM3	S10	2D	2C	3D	3C	4D	COL	5D	5C		T4	4G	1C	1D
COM2	S9	2E	2G	3E	3G	4E	4C	5E	5G	T	T3	4K	1G	1E
COM1	S8	2F	2B	3F	3B	4F	4B	5F	5B	S7	T2	4A	1B	1F
COM0		2A	S2	3A	S3	S4	P1	P2	P3	S6	T1	S5	S1	1A

四.引脚特性:

引脚号	引脚名称	级　别	引　脚　功　能　描　述
1	VLCD	5.0V	LCD 输入电压
2	VSS	0V	电源地
3	OSC	H/L	外部时钟
4	VDD	5.0V	电源输入
5	RSTB	H/L	复位，低有效
6	SYNC	H/L	级联同步输入输出
7	SCL	H/L	锁存
8	SDA	H/L	数据

五.电气特性:

1.限定参数:

项　　目	名称	值	单位	备 注
Operating Voltage	VDD	+4.8 to +5.2	V	*1
Supply Voltage	VEE	+4.8 to +5.2	V	*2

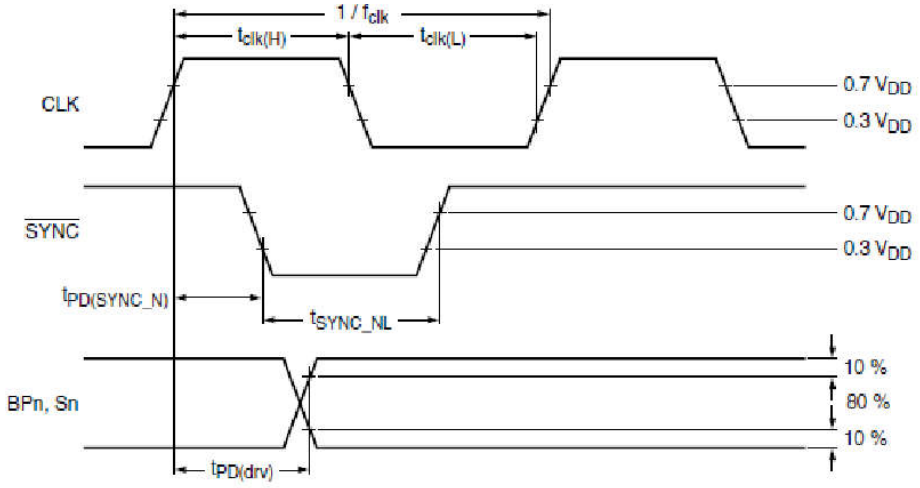
项　　目	名称	值	单位	备 注
Operating Temperature	T_{OPR}	-10 to +60	℃	
Storage Temperature	T_{STG}	-20 to +70	℃	

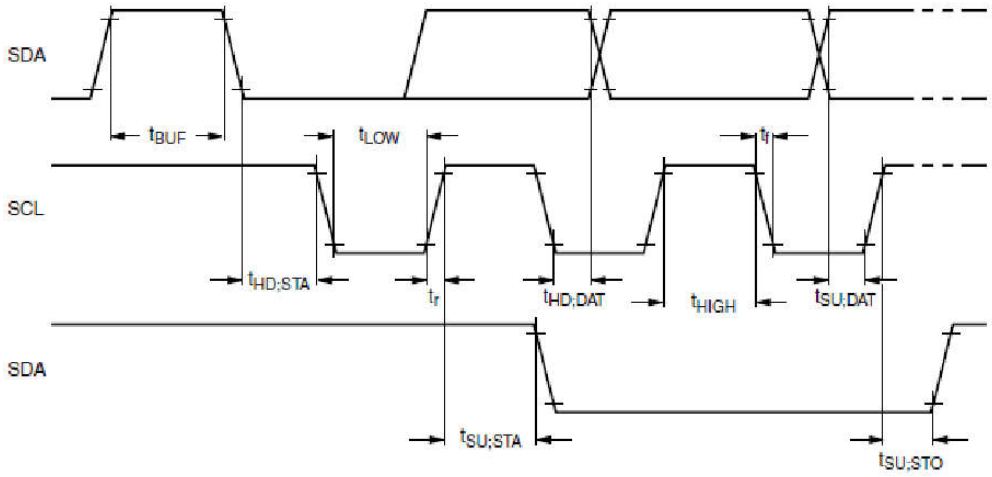
2. 直流特性:（VDD=+5.0V，VSS=0V， VLCD=5.0V，Ta=-10～+60℃）

项　　目	名称	测试条件	Min	Typ	Max	单位	备注
Input High Voltage	V_{IH}	-	2.5	-	5.5	V	*1
Input Low Voltage	V_{IL}	-	0	-	0.6	V	*1
Output High Voltage	V_{OH}	I_{OH}=-500uA	2.4	-	-	V	*2
Output Low Voltage	V_{OL}	I_{OL}=0.5mA		-	0.6	V	*2
Input Leakage Current	I_{LKG}	V_{IN}=VSS～VDD	-1.0	-	1.0	uA	*3
Three-state(OFF) input Current	I_{TSL}	V_{IN}=VSS～VDD	-3.3	-	3.3	uA	*4
Operating Current	I_{DD1}	During Display	-	-	0.5	mA	*5
	I_{DD2}	During Access			1	mA	*5

六. 时序特性:

时序图:





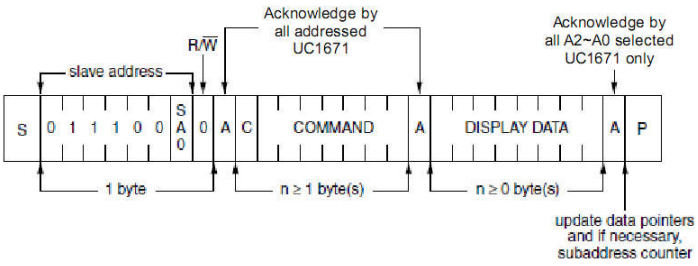
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Clock						
$f_{CLK\ (INT)}$	Internal clock frequency	[1]	-25%	1536 1970 **2640** 4800	+25%	Hz
$f_{CLK\ (EXT)}$	External clock frequency		800	–	9600	Hz
$f_{FR\ (INT)}$	Internal clock Frame frequency		-25%	64 82 **110** 220	+25%	Hz
$f_{FR\ (EXT)}$	External clock Frame frequency		33	–	400	
$t_{CLK(H)}$	High-level clock time		60	–	–	uS
$t_{CLK(L)}$	Low-level clock time		60	–	–	uS
Synchronization						
$t_{PD(SYNC_N)}$	$\overline{SYNC}$ propagation delay		–	30	–	nS
t_{SYNC_NL}	$\overline{SYNC}$ low time		1	–	–	uS
$t_{PD(DRV)}$	Driver propagation delay	V_{LCD}=5V [2]	–	–	30	uS

I^2C bus timing [3]						
f_{SCL}	SCL clock frequency	pin SCL	–	–	400	kHz
t_{LOW}	LOW period of the SCL clock	pin SCL	1.3	–	–	uS
t_{HIGH}	HIGH period of the SCL clock	pin SCL	0.6	–	–	uS
$t_{SU;DAT}$	Data set-up time	pin SDA	100	–	–	nS
$t_{HD;DAT}$	Data hold time	pin SDA	0	–	–	nS
t_{BUF}	Bus free time between STOP & START	pins SCL and SDA	1.3	–	–	uS
$t_{SU;STO}$	Set-up time from STOP condition		0.6	–	–	uS
$t_{HD;STA}$	Hold time (repeated) START condition		0.6	–	–	uS
$t_{SU;STA}$	Set-up time for a repeated START condition		0.6	–	–	uS
t_R	Rise time of both SDA and SCL signals	F_{SCL}=400kHz	–	–	0.3	uS
		F_{SCL}<125Hz	–	–	1.0	
t_F	Fall time of both SDA and SCL signals		–	–	0.3	uS
C_B	Capacitive load for each bus line		–	–	400	pF
$t_{W(SPIKE)}$	Spike pulse width	On the I^2C bus	–	–	50	nS

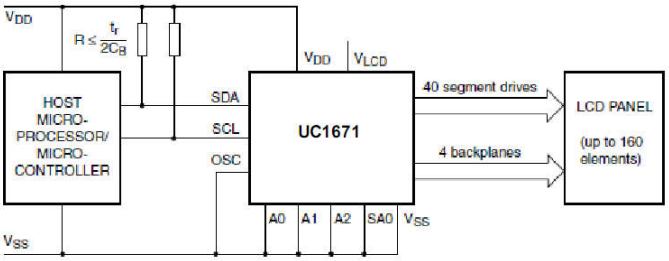
Note: The rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS.

[1] Typical output duty factor: 50 % measured at the CLK output pin.
[2] Not tested in production.
[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of Vss to V_{DD}.

I^2C-bus Protocol



Typical System Configuration



The resistance of the power lines must be kept to a minimum.

七. 指令说明：

COMMAND TABLE

D7-D0: C: Continuation bit. C=0: last control byte in the transfer; next byte will be regarded as display data.
C=1: control byte continues; next byte will be a command, too.

#	Command	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Mode-set	C	1	0	PS	E	B	M1	M0	Set Display Mode	{PS, E, B, M}=0h
2	Load-data-pointer	C	0	P5	P4	P3	P2	P1	P0		P[5:0]=00h
3	Frame-Rate-select	C	1	1	0	1	1	FR1	FR0	Select Frame Rate	10b
4	Device-select	C	1	1	0	0	A2	A1	A0	Select Device	000b
5	Bank-select	C	1	1	1	1	0	I	O	Select Bank	{I, O}=00b
6	Blink-select	C	1	1	1	0	A	BF1	BF0	Select Blink Mode	{A, BF}=000b

COMMAND DESCRIPTION

D7-D0: C: Continuation bit. C=0: last control byte in the transfer; next byte will be regarded as display data.
C=1: control bytes continue; next byte will be a command too.

(1) Mode-Set

Action	D7	D6	D5	D4	D3	D2	D1	D0
Set mode	C	1	0	PS	E	B	M1	M0

PS: Display power saving mode switch.

0: Internal clock ON 1: Internal clock OFF, (for Power Saving).

The power saving mode is ON only when the OSC pin is Low and the display is disabled (E=0).

E: Display status

0: Display disabled (blank) 1: Display enabled

B: LCD bias configuration

0: 1/3 bias 1: 1/2 bias

M[1:0]: LCD drive mode selection

00b: 1:4 multiplex; BP0~3 01b: static; 1 backplane; BP0

10b: 1:2 multiplex; BP0~1 11b: 1:3 multiplex; BP0~2

(2) Load-Data-Pointer

Action	D7	D6	D5	D4	D3	D2	D1	D0
Load data pointer	C	0	P5	P4	P3	P2	P1	P0

P[5:0]: Display RAM addresses. Value range: **00 0000**b~10 0111b, that is 0~39 in decimal. The value will be transferred to the data pointer to define one of 40 Display RAM addresses.

(3) Frame-Rate-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select Frame Rate	C	1	1	0	1	1	FR1	FR0

FR[1:0]: Frame rate 00b: 64Hz 01b: 82Hz **10b: 110Hz** 11b: 200Hz

(4) Device-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select Device	C	1	1	0	0	A2	A1	A0

A[2:0]: 3-bit binary value of 0 to 7 (default **000**b), transferred to the sub-address counter to define one of 8 hardware sub-addresses.

(5) Bank-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select RAM I/O	C	1	1	1	1	0	I	O

I: Input bank selection **0: RAM bit 0 (RAM bits 0 and 1)** 1: RAM bit 2 (RAM bits 2 and 3)

	Storage of Arriving Display Data	
	Static	1:2 multiplex
I=0	RAM bit 0	RAM bits 0 and 1
I=1	RAM bit 2	RAM bits 2 and 3

O: Output bank selection **0: RAM bit 0 (RAM bits 0 and 1)** 1: RAM bit 2 (RAM bits 2 and 3)

	Retrieval of LCD Display Data	
	Static	1:2 multiplex
O=0	RAM bit 0	RAM bits 0 and 1
O=1	RAM bit 2	RAM bits 2 and 3

This command has no effect in 1:3 or 1:4 multiplex drive mode.

D7-D0: C: Continuation bit. C=0: last control byte in the transfer; next byte will be regarded as display data.
C=1: control bytes continue; next byte will be a command too.

(6) Blink-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select blink	C	1	1	1	0	A	BF1	BF0

A: Blink mode selection

0: Normal blinking. Normal blinking can only be selected when multiplex drive mode=1:3 or 1:4.

1: Blinking by alternating display RAM banks
Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

BF[1:0]: Blink frequency selection

00b: OFF 01b: Blink mode 1 10b: Blink mode 2 11b: Blink mode 3

See the Blink Frequency table for detailed description about each blink mode.